REMARKS

Applicants have amended claims 1-4 and 6-8 to improve English usage without changing claim scope. Claim 5 has been amended to reflect the disclosure of paragraph [0047] of the specification.

The Examiner requested that FIGS. 1 and 2 be labeled as "Prior Art." Applicants have amended the drawings accordingly.

Claims 1-8 have been rejected under 35 USC 112, second paragraph, as indefinite because claim 1 recited "relative speed" without a standard for the relativity and included the expression "a silicon oxide film formed on the surface is previously removed" which made the order of the etching of the silicon oxide and silicon uncertain. Claim 1 as amended recites "a speed relative to the semiconductor wafer" and states that silicon is etched after the silicon oxide is removed. Accordingly, this indefiniteness rejection should be withdrawn.

Claim 1 has been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 5,953,578 (Lee). Applicants respectfully traverse this rejection.

Claim 1 as amended recites removing the silicon oxide film so that silicon is exposed on the surface of the semiconductor wafer and etching the exposed silicon by moving the nozzle that applies the activated species gas at a controlled speed relative to the semiconductor wafer. Because the silicon oxide film, which has a lower etching rate than silicon, is removed from the surface of the semiconductor wafer, the exposed silicon can be etched according to the "position-thickness data" obtained beforehand. See, for example, paragraph [0047] of the specification.

The Examiner contends that Lee's ion beam etching method shown in FIG. 1 of Lee performs the claimed removal of the silicon oxide film to expose silicon on the surface of the semiconductor wafer. Specifically, the Examiner points to column 2, lines 17-23, of Lee for this teaching. However, with respect to the removal of the silicon oxide film this passage of Lee only states, "The gases fed to the inlet 13 etch the oxide on the wafer where the beam falls." Lee does not teach that the oxide is removed to expose silicon on the surface of the semiconductor wafer as claimed. In fact, Lee is directed to providing a polishing method alternative to chemical-

mechanical polishing (CMP). See column 1, lines 18-30, of Lee. Persons of ordinary skill in the art would have known that CMP is used to flatten a device element formed on a semiconductor wafer, such as a silicon oxide film and a silicon nitride film, but not to remove the device element completely to expose the silicon surface underneath the device element.

Lee also states at column 1, lines 61-63, "The principle of this invention is to use chemical ion beam etching to remove unevenness portions of an IC surface so that the surface is planarized." (Emphasis added) Accordingly, Lee's ion beam etching flattens device elements of an IC formed on the surface of the silicon substrate and does not remove such device elements completely to expose the silicon substrate as claimed. On the other hand, the claimed local dry etching method flattens the silicon substrate itself.

The rejection of claim 1 under 35 USC 102(b) on Lee should be withdrawn because Lee does not teach or suggest the claimed removal of the silicon oxide film to expose silicon on the surface of the semiconductor.

Claims 1-8 have been rejected under 35 USC 103(a) as unpatentable over Japanese Patent Application Publication No. 2001-144072 (Yanagisawa) in view of the Background of the Invention section of the specification. Applicants respectfully disagree.

The Examiner contends that the translated abstract of Yanagisawa discloses the claimed removal of the silicon oxide film explained above. Applicant respectfully disagree. Yanagisawa's abstract states, "By filing this oxygen active species G1 in a chamber 1, … an oxide film is formed over the whole surface of the silicon wafer W." What Yanagisawa teaches is to form an oxide film on a wafer after the etching of the wafer for the protection of etched surface of the wafer. Yanagisawa says nothing about removing the oxide formed on the wafer surface. For the Examiner's convenience, applicants have made a English translation of Yanagisawa using the automated translation tool provided at the Japanese Patent Office web site and attach the translation to this amendment. Paragraph [0006] of the translation, which includes a statement, "Since the oxide film is formed in the silicon wafer of this configuration, when a

when a silicon wafer is put into air, by it, a silicon wafer does not adsorb the quality of an impurity in air," provides an additional basis for applicants' argument.

The rejection of claims 1-8 under 35 USC 103(a) over Yanagisawa and the Background section should be withdrawn because Yanagisawa and the Background section together do not teach or suggest the claimed removal of the silicon oxide film.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **506212001100**.

Respectfully submitted,

Dated: July 29, 2005

By _____

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In the Drawings:

The attached sheet of drawings includes changes to FIGS. 1 and 2. This sheet replaces the original sheet of FIGS. 1 and 2.

Attachment: Replacement sheet